REMARKS

Claims 1-24 are pending in the application. No claims have been amended.

Claim Rejections – 35 U.S.C. §103(a)

The Examiner rejected claims 1-24 under 35 USC 102(e) as being unpatentable over Devic (U.S. Patent No. 6,054,993) in view of Shirman et al (U.S. Patent No. 5,550,960). Applicant respectfully disagrees with the Examiner's rejection. In particular, both Devic and Shirman fail to teach or suggest a "logical binding is provided between the internal texture coordinate sets used by the graphics device and plurality of texture coordinates associated with vertices of three dimensional objects," as claimed or similar claimed.

The present invention provides a logical binding between the *internal* texture coordinate sets used by a graphics device and *externally* stored (i.e., within the system memory) vertex texture coordinates or a default value. This logical mapping provides substantial flexibility with respect to the use, ordering and possibly replication of vertex texture coordinates. As noted in the specification on page 11, line 7 to page 12, line 2:

> Accordingly, by utilizing these logical bindings, specific vertex texture coordinate sets that are present in the vertex data array may be ignored. This may better support the operation of the Direct 3D API, which does not prevent unused texture coordinate sets from being presented to the graphics driver or stored in the vertex buffers. This allows applications to keep one vertex database (with possibly more texture coordinates sets than the hardware can use at any point in time) and then employ a multipass rendering algorithm where a subset of the coordinate sets may be used in each pass.
>
> The logical binding functionality may allow multiple internal texture coordinate sets to be bound to the same vertex texture coordinate sets. This may be useful for replicating vertex texture coordinate sets in order to apply different attributes (e.g., texture address controls, texture coordinate transforms, etc.) to the same texture coordinate set for use with different texture mappings. This may be useful for matching the Direct 3D API semantics of associating these controls with texture stages versus texture coordinate sets.
>
> The logical bindings also allow the vertex texture coordinate sets to be used in a random (versus strictly sequential) fashion.
>
> Embodiments of the present invention provide advantages over graphic devices that support a fixed (i.e., implied) binding between the vertex texture coordinate set and the internal texture coordinate sets. That is, embodiments of the present invention permit vertex texture coordinates to be ignored, permit vertex texture coordinates to be replicated, permit vertex texture coordinates to be used in random order and permit the association of a default value to a

> texture coordinate set. Without this flexibility, the graphics driver would be generate a second, rearranged copy of the vertex data, which adds additional memory bandwidth requirements and software overhead and thus reduces the system performance.

Both Devic and Shirman fail to teach or suggest a logical binding provided between the internal texture coordinate sets used by the graphics device and plurality of texture coordinates associated with vertices of three dimensional objects. In fact, Devic teaches away in that it supports a fixed (i.e. implied) binding between vertex and internal texture coordinate sets. This requires the graphics driver to generate a second, rearranged copy of the vertex data (adding software overhead and thus reducing system performance).

Shirman also fails to disclose a logical binding between internal texture coordinate sets used by the graphics device and texture coordinates associated with vertices of three dimensional objects. The present invention provides, for a graphics device supporting multiple texture mappings, a logical binding between the internal texture coordinate sets used by the device, and the externally stored vertex coordinates or a default value. This logical mapping provides substantial flexibility with respect to the use, ordering, and possible replication of vertex texture coordinates. Without this flexibility, the graphics driver would typically for example be required to generate a second, rearranged copy of the vertex data at the cost of memory footprint, and additional driver overhead, complexity and thus lower system performance.

Shirman addresses something fundamentally different from the claimed invention. In particular, as noted in column 3, lines 60-67:

> The process of the present invention is described generally with reference to FIG. 2. The object is described in MC space 105 or, alternately, world coordinate (WC) space. The texture map is defined in TC space 120. The object is subsequently rendered and displayed in the DC space 130. A parameterization process "P" is used to bind the object 110 to the PC space 115. This process is performed once for an object and is view independent and texture independent. A mapping is then performed between the TC space 120 and PC space 115. This mapping is referred to herein as the .tau. mapping. The .tau. mapping is subsequently used to apply the texture map to the object 110 in the display coordinate space 130.

In particular, the binding in Shirman is directed to binding the object to the PC space. This has nothing to do with the claimed logical binding between the internal texture coordinate sets used by a graphics device and externally stored (i.e., within the system memory) vertex texture coordinates or a default value. Furthermore, Shirman teaches away in that it supports a fixed (i.e. implied) binding between vertex and internal texture coordinate sets. See Column 4, lines 1-5. There is nothing to indicate a logical mapping that provides flexibility with respect to the use, ordering, and possible replication of vertex texture coordinates. There is also no motivation to combine the two references.

It is therefore respectfully requested that the Examiner withdraw his rejection of the pending claims.

CONCLUSION

In view of the foregoing, it is respectfully asserted that all of the claims pending in this patent application are in condition for allowance.

The required fee for a three month extension of time is enclosed. Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666.

If the Examiner has any questions, he is invited to contact the undersigned at (323) 654-8218. Reconsideration of this patent application and early allowance of all the claims is respectfully requested.

Respectfully submitted,

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CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 19, 2004

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Marilyn Bass August 19, 2004